



# PH7030L

## N-channel TrenchMOS™ logic level FET

Rev. 04. — 7 March 2005

Product data sheet

### 1. Product profile

#### 1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS™ technology.

#### 1.2 Features

- Low thermal resistance
- Logic level gate drive
- S08 equivalent area footprint
- Low on-state resistance.

#### 1.3 Applications

- DC-to-DC converters
- Portable appliances
- Switched-mode power supplies
- Notebook computers.

#### 1.4 Quick reference data

- $V_{DS} \leq 30\text{ V}$
- $I_D \leq 68\text{ A}$
- $R_{DSon} \leq 7.9\text{ m}\Omega$
- $P_{tot} \leq 62.5\text{ W}$ .

### 2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source	<p>SOT669 (LFPAK)</p>	<p>mbb076</p>
4	gate		
mb	mounting base; connected to drain		

### 3. Ordering information

**Table 2: Ordering information**

Type number	Package		Version
	Name	Description	
PH7030L	LFAK	plastic single-ended surface mounted package; 4 leads	SOT669

### 4. Limiting values

**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

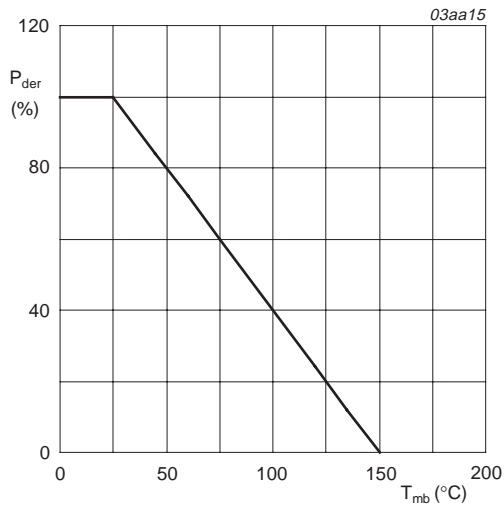
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
$V_{GS}$	gate-source voltage (DC)		-	$\pm 20$	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ <a href="#">Figure 2</a> and <a href="#">3</a>	-	68	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ <a href="#">Figure 2</a>	-	43	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ <a href="#">Figure 3</a>	-	220	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Figure 1</a>	-	62.5	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C

#### Source-drain diode

$I_S$	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	52	A
$I_{SM}$	peak source (diode forward) current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	150	A

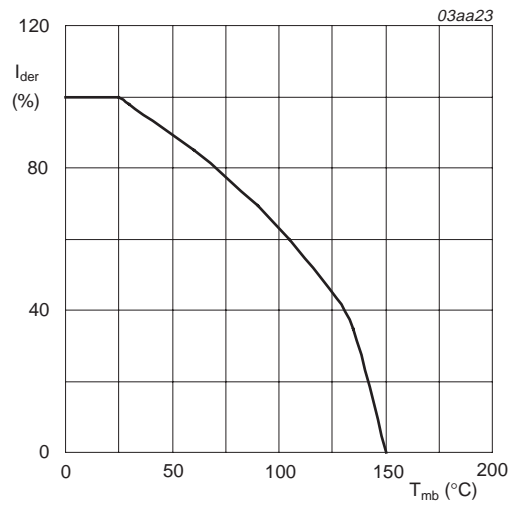
#### Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 33.9\text{ A};$ $t_p = 0.15\text{ ms}; V_{DD} \leq 30\text{ V}; V_{GS} = 10\text{ V};$ starting at $T_j = 25\text{ °C}$	-	115	mJ
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$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

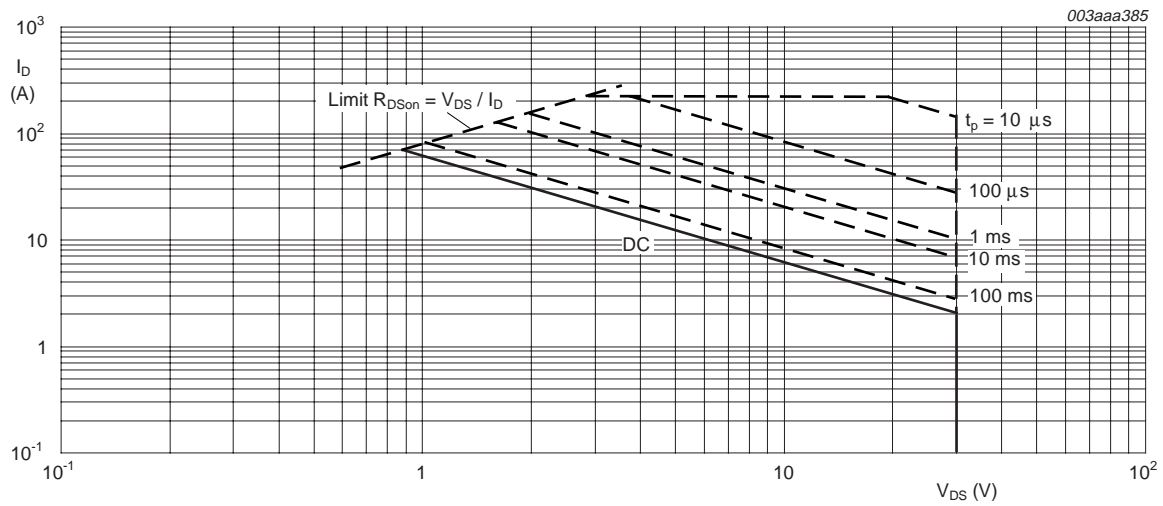
Fig 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25^\circ\text{C}$ ;  $I_{DM}$  is single pulse;  $V_{GS} = 10\text{ V}$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

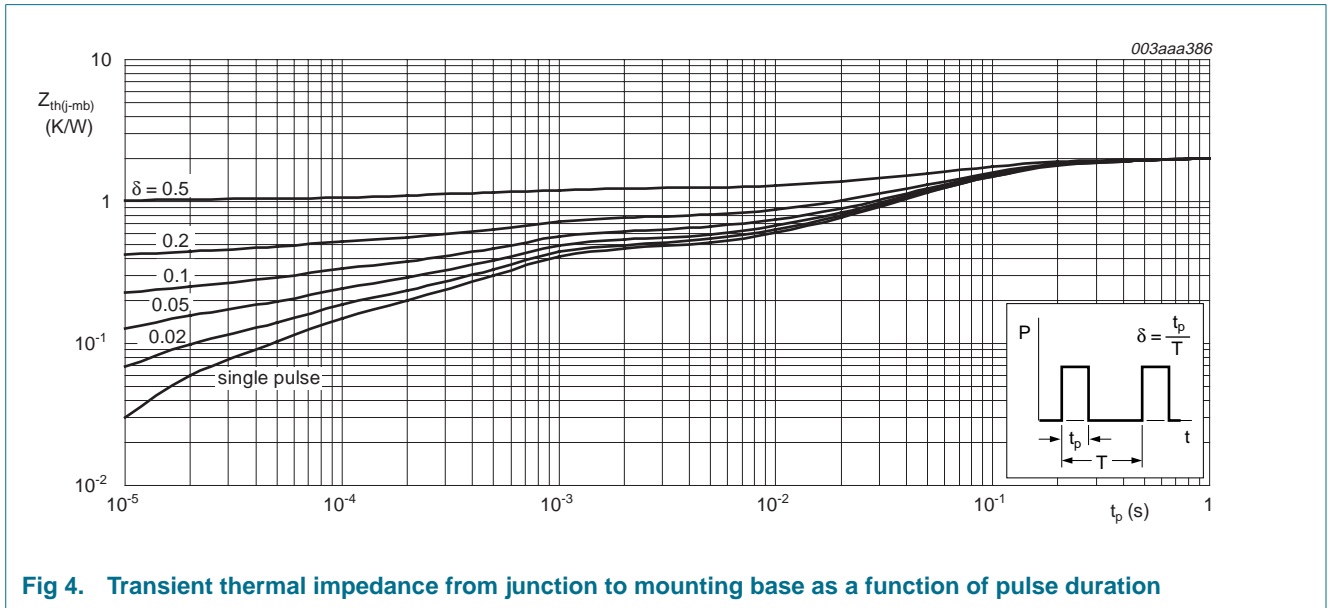


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Static characteristics</b>							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V	30	-	-	V	
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; <a href="#">Figure 9</a>					
		T <sub>j</sub> = 25 °C	1	1.5	2	V	
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V	T <sub>j</sub> = 150 °C	0.6	-	-	V
			T <sub>j</sub> = 25 °C	-	0.06	1	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±15 V; V <sub>DS</sub> = 0 V	-	20	100	nA	
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; <a href="#">Figure 7</a> and <a href="#">8</a>	T <sub>j</sub> = 25 °C	-	6.9	7.9	mΩ
			T <sub>j</sub> = 150 °C	-	11.7	13.2	mΩ
			V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 10 A;	-	9.6	11	mΩ
			V <sub>GS</sub> = 5 V; I <sub>D</sub> = 10 A;	-	8.7	10	mΩ
<b>Dynamic characteristics</b>							
Q <sub>g(tot)</sub>	total gate charge	I <sub>D</sub> = 20 A; V <sub>DS</sub> = 10 V; V <sub>GS</sub> = 5 V; <a href="#">Figure 13</a>	-	12	-	nC	
Q <sub>gs</sub>	gate-source charge		-	4.1	-	nC	
Q <sub>gd</sub>	gate-drain (Miller) charge		-	3.2	-	nC	
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 10 V; f = 1 MHz; <a href="#">Figure 11</a>	-	1362	-	pF	
C <sub>oss</sub>	output capacitance		-	544	-	pF	
C <sub>rss</sub>	reverse transfer capacitance		-	260	-	pF	
t <sub>d(on)</sub>	turn-on delay time	V <sub>DD</sub> = 10 V; I <sub>D</sub> = 10 A;	-	24	-	ns	
t <sub>r</sub>	rise time	V <sub>GS</sub> = 4.5 V; R <sub>G</sub> = 4.7 Ω	-	38	-	ns	
t <sub>d(off)</sub>	turn-off delay time		-	34	-	ns	
t <sub>f</sub>	fall time		-	21	-	ns	
<b>Source-drain diode</b>							
V <sub>SD</sub>	source-drain (diode forward) voltage	I <sub>S</sub> = 10 A; V <sub>GS</sub> = 0 V; <a href="#">Figure 12</a>	-	0.81	1.2	V	
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>R</sub> = 20 V	-	11	-	ns	

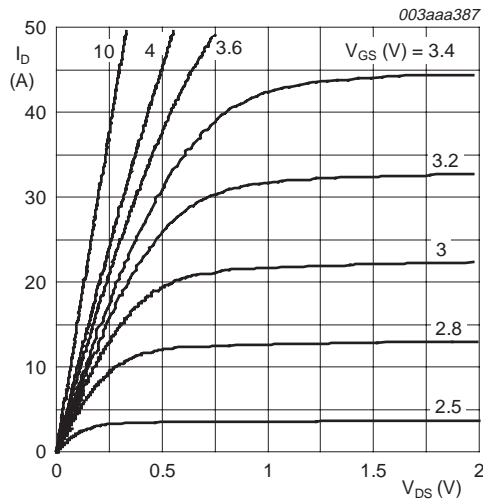


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

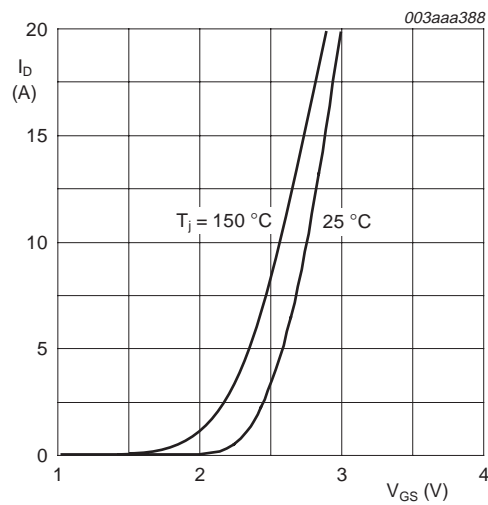


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

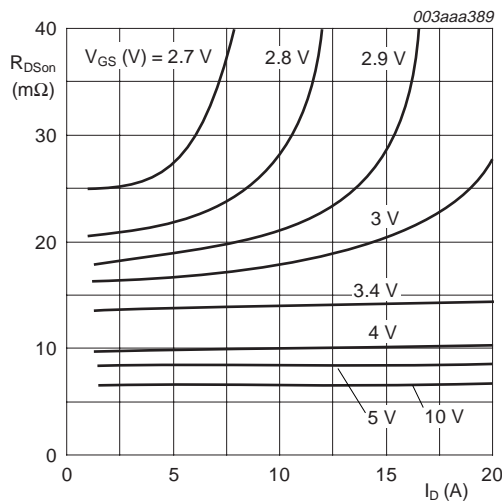
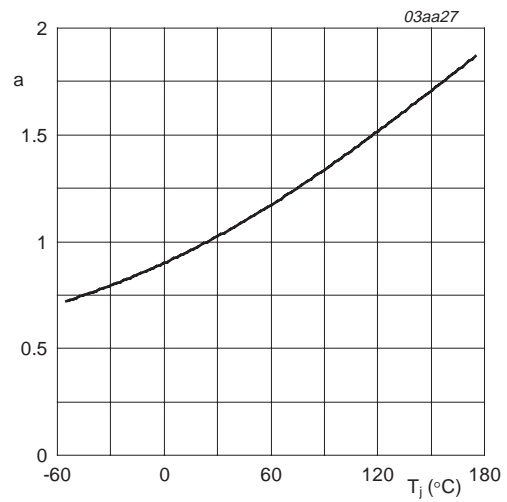
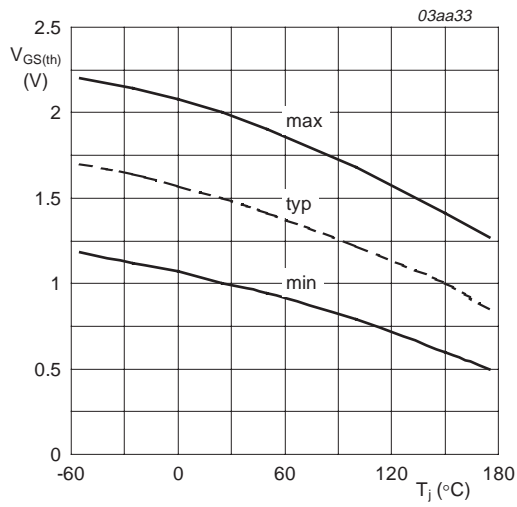


Fig 7. Drain-source on-state resistance as a function of drain current; typical values



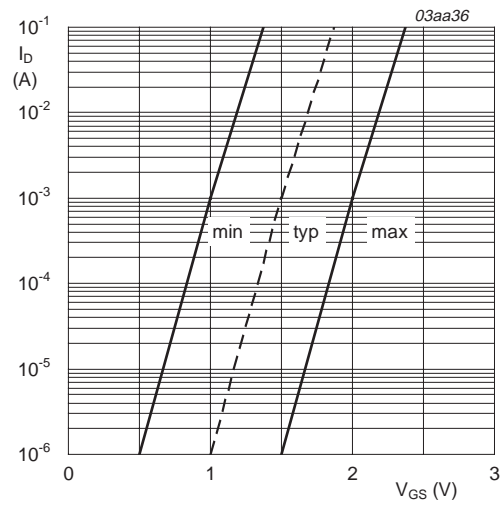
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



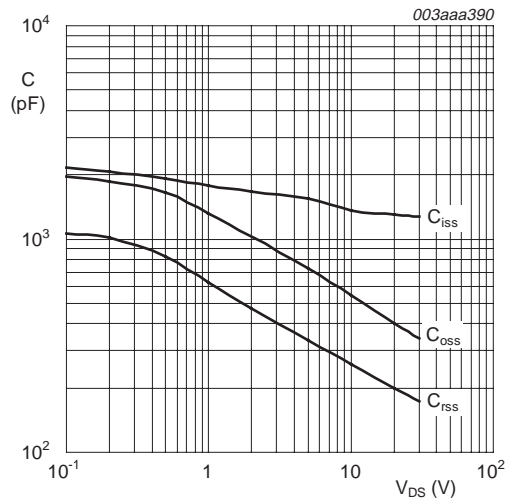
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



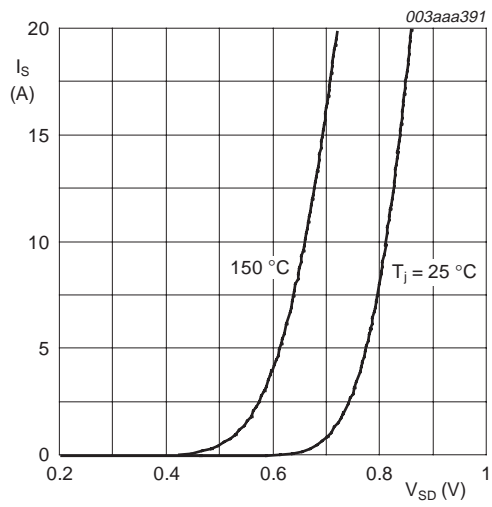
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



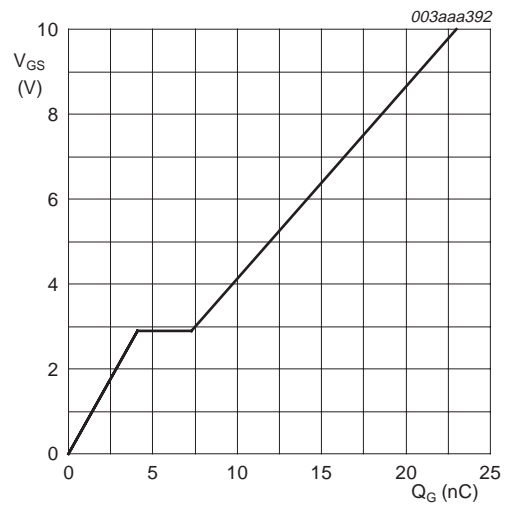
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25\text{ °C}$  and  $150\text{ °C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**



$I_D = 20\text{ A}$ ;  $V_{DD} = 10\text{ V}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values**



7. Package outline

Plastic single-ended surface mounted package (LPAK); 4 leads

SOT669

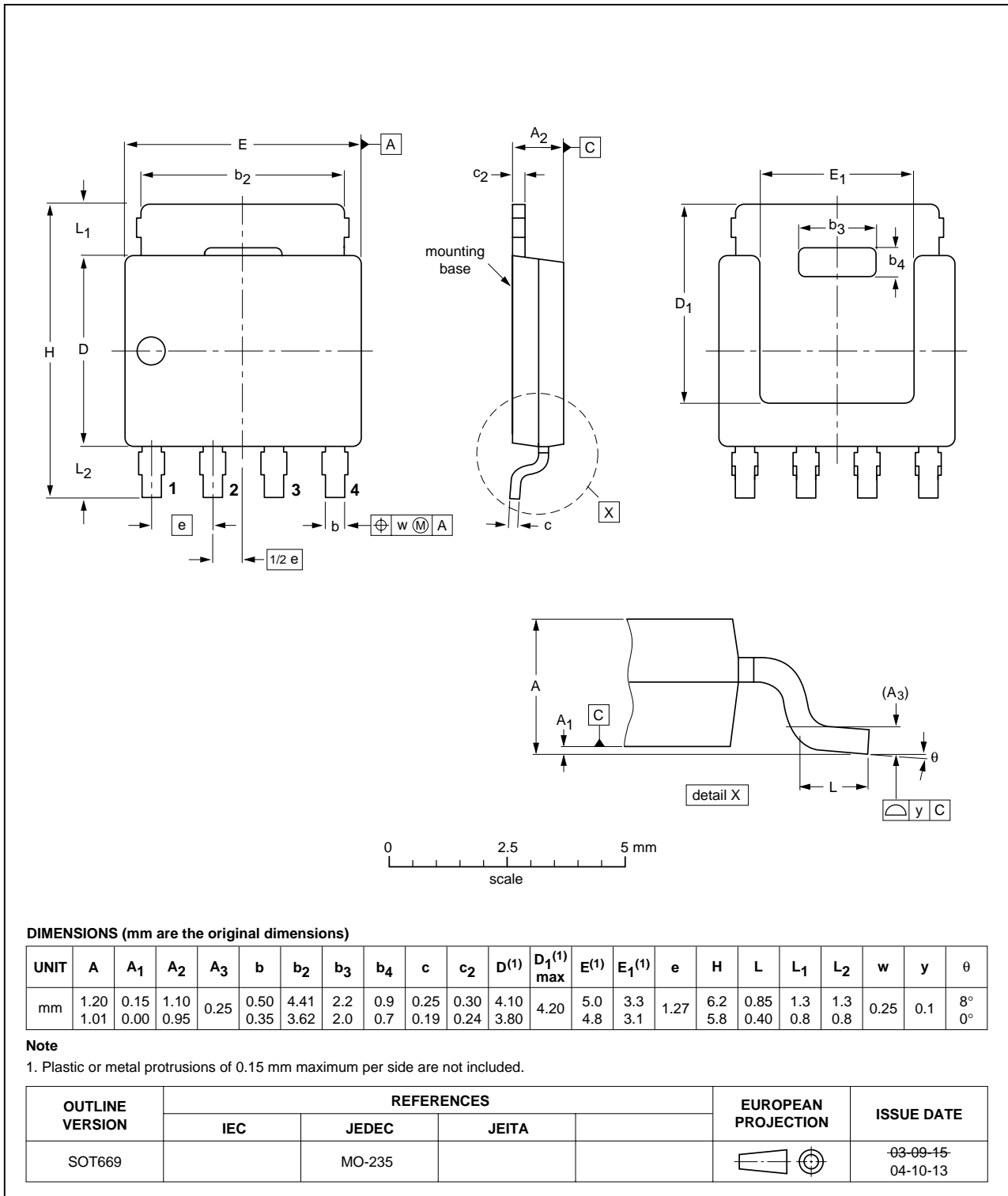


Fig 14. Package outline SOT669 (LPAK)

## 8. Revision history

**Table 6: Revision history**

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PH7030L_4	20050307	Product data sheet	-	9397 750 14206	PH7030L-03
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li> <li><a href="#">Table 5 “Characteristics”</a>: <math>R_{DSon}</math> data added.</li> </ul>				
PH7030L-03	20040304	Product data		9397 750 12944	PH7030L-02
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 5 “Characteristics”</a>, <math>t_r</math> data revised.</li> </ul>				
PH7030L-02	20030918	Product data		9397 750 11946	PH7030L-01
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 3 “Ordering information”</a> added.</li> <li><a href="#">Section 1.4 “Quick reference data”</a> and <a href="#">Table 3 “Limiting values”</a>, <math>I_D</math> data revised.</li> <li><a href="#">Section 1.4 “Quick reference data”</a> and <a href="#">Table 5 “Characteristics”</a>, <math>R_{DSon}</math> data revised.</li> <li><a href="#">Section 4 “Limiting values”</a>, <math>V_{GS}</math> data revised.</li> <li><a href="#">Table 5 “Characteristics”</a>, <math>Q_{g(tot)}</math>, <math>Q_{gs}</math>, <math>Q_{gd}</math>, and <math>V_{SD}</math> data revised.</li> <li><a href="#">Figure 3</a>, <a href="#">4</a>, <a href="#">7</a>, <a href="#">8</a> and <a href="#">13</a> updated.</li> </ul>				
PH7030L-01	20030502	Product data	-	9397 750 11405	-

## 9. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## 14. Contents

<b>1</b>	<b>Product profile</b> . . . . .	<b>1</b>
1.1	General description . . . . .	1
1.2	Features . . . . .	1
1.3	Applications . . . . .	1
1.4	Quick reference data . . . . .	1
<b>2</b>	<b>Pinning information</b> . . . . .	<b>1</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>
<b>4</b>	<b>Limiting values</b> . . . . .	<b>2</b>
<b>5</b>	<b>Thermal characteristics</b> . . . . .	<b>4</b>
<b>6</b>	<b>Characteristics</b> . . . . .	<b>5</b>
<b>7</b>	<b>Package outline</b> . . . . .	<b>9</b>
<b>8</b>	<b>Revision history</b> . . . . .	<b>10</b>
<b>9</b>	<b>Data sheet status</b> . . . . .	<b>11</b>
<b>10</b>	<b>Definitions</b> . . . . .	<b>11</b>
<b>11</b>	<b>Disclaimers</b> . . . . .	<b>11</b>
<b>12</b>	<b>Trademarks</b> . . . . .	<b>11</b>
<b>13</b>	<b>Contact information</b> . . . . .	<b>11</b>



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